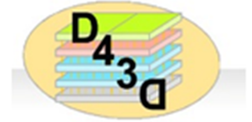

LETI D43D WORKSHOP

DESIGN FOR 3D

JUNE 26-27, 2017
GRENOBLE, FRANCE

D43D WORKSHOP

26-27 June, 2017, Minatec, Grenoble

9th Workshop on Design for 3D Silicon Integration

Monday 26 June - Day 1		
12:30 - 14:00	**Welcome Lunch**	
13:45 - 14:00	**Opening Session**	**Pascal Vivet**, CEA-LETI, France
Session 1	**3D Memory Devices**	
	Chair: Jean-Francois Roy, UPMEM, France	
14:00 - 14:30	**Non Volatile Memory: a wide spectrum of potential solutions**	**Etienne Nowack**, CEA-LETI, France
14:30 - 15:00	**3D Memory : Patent Landscape Analysis**	**Audrey Bastard**, KNOWMADE, France
15:00 - 15:30	**Power, Heat, Reliability: A 3D Physical Design Perspective**	**Aida Todri**, LIRMM, France
15:30 - 16:00	**COFFEE BREAK**	
Session 2	**3D Emerging Memories and New Architecture Paradigms**	
	Chair : Bastien Giraud, CEA-LETI, France	
16:00 - 16:30	**Abundant-Data Computing: The N3XT 1,000X**	**Subhasish Mitra**, Stanford University, France
16:30 - 17:00	**Novel 3D technologies for the transition to cognitive systems**	**Bert Offrein**, IBM Zurich, Switzerland
17:00 - 17:30	**3D Memories: Now and Then!**	**Christian Weiss**, Univ. of Kaiserslautern, Germany

Tuesday 27 June - Day 2		
Session 3	**3D Technology Landscape and Advanced Imagers**	
	Chair : Didier Lattard, CEA-LETI, France	
9:00 - 9:30	**Evolution and adoption of 3D TSV and 2.5D technology : From high performance to consumers applications**	**Emilie Jolivet,** YOLE, France
9:30 - 10:00	**Advanced 3D technologies for innovative 3D architecture**	**S. Cheramy**, CEA-LETI, France
10:00 - 10:30	**Smart imager: Computer vision integration with 3D stack**	**Jerome Chossat,** STMicroelectronics, France
10:30 - 11:00	**COFFEE BREAK**	
Session 4	**3D for High Performance Computing**	
	Chair : Patrick Blouet, STMicroelectronics, France	
11:00 - 11:30	**Emerging architectures for computing with 3D silicon integration**	**Denis Dutoit**, CEA-LETI, France
11:30 - 12:00	**2.5D/3D Systems with Silicon Photonic NoCs: Efficient Thermal Management, Opportunities, and Challenges**	**Ayse Coskun**, University of Boston, USA
12:00 - 12:30	**In-memory Computing with Majority RRAM Operations**	**Pierre-Emmanuel Gaillardon,** University of Utah, USA
12:30 - 14:00	**LUNCH BREAK**	
Session 5	**Monolithic 3D : from Technology to Advanced Design**	
	Chair: Sébastien Thuriès, CEA-LETI, France	
14:00 - 14:30	**Technological status of monolithic 3D**	**Perrine Batude,** CEA-LETI, France
14:30 - 15:00	**Power, performance and area benefits of monolithic 3D-IC for equivalent Moore's Law scaling**	**Shidhartha Das,** ARM, UK
15:00 - 15:30	**On Efficient Ways to Use Commercial 2D IC EDA Tools to Build Commercial Quality Monolithic 3D IC Designs**	**Sung Kyu Lim,** Georgia Institute of Tech, USA
15:30 - 16:00	**COFFEE BREAK**	
Session 6	**3D Design and Tools**	
	Chair : Sung Kyu Lim, Georgia Institute of Tech, USA	
16:00 - 16:25	**Design Considerations and Noise Issues for Heterogeneous Contactless 3-D ICs**	**Vasilis Pavlidis,** Manchester University, UK
16:25 - 16:50	**Chip-to-chip communication on interposer based systems**	**Fabian Hopsch,** Fraunhofer Institute, Germany
16:50 - 17:10	**Modeling Challenges in Electrical Design of 3DIC based Systems**	**Dusan Petranovic,** Mentor Graphics, USA
17:10 - 17:30	**HANOI Whiteboard Flow: the Seed for 2.5D-IC Implementation**	**Anna Fontanelli**, Monozukiri, Italy